

# VITA<sup>™</sup> 68 standardizes the VPX<sup>™</sup> Compliance Channel to allow a common backplane design to support multiple fabric protocols

By Bob Sullivan  
Hybricon

As the industry moves to higher serial fabric baud rates on VPX, the risk of signal integrity interoperability issues becomes increasingly severe. In order to deliver on the VITA 65 OpenVPX<sup>™</sup> promise of interoperability, signal integrity requirements need to be independently defined for both backplanes and plug-in modules. The VPX family of standards does not currently define any signal integrity requirements for fabric connections across backplanes. At the current rates of 3.125 Gbaud and below, good industry design practices have minimized these problems, but this is not a tenable long term approach at higher rates. VITA 65 OpenVPX adds PCIe and SRIO Gen 2 rates of 5.0 Gbaud and 6.25 Gbaud in backplane profiles as well as module profiles, and these higher rates are being added to the VITA 46 VPX fabric dot specs for PCIe and SRIO as well. The VITA 65 community has determined that a compliance channel standard is needed in order to avoid signal integrity interoperability problems, particularly at the higher baud rates, and VITA 65 compliance mandates that products comply with VITA 68 signal integrity requirements.

VITA 68 defines a VPX compliance channel including common backplane performance criteria required to support multiple fabric types across a range of defined baud rates. This allows backplane developers to design a backplane that can support the required bit error rates (BER) for multiple fabric types. This also allows module developers to design plug-in modules that are interoperable with other modules when used with a compliant backplane. Based on VITA 68, backplane and module vendors will be able design compliant, interoperable hardware independently.

## **VITA 68 approach**

VITA 68 defines a VPX compliance channel based on the channel performance methodology and metrics that are used in IEEE 802.3-2008 for 1000BASE-KX, 10GBASE-KX4, and 10GBASE-KR for up to 10.3 Gbaud per pair.

This methodology is comprehensive, and defines a number of frequency domain channel parameters that can be adapted to the PCIe and SRIO Gen 1 and Gen 2 baud rates. Key channel parameters are:

- Insertion Loss (IL): Defined as the magnitude, expressed in decibels, of the differential SDD21 response of the channel
- Fitted Attenuation (A): Defined to be least mean squares line fit to the insertion loss computed over a specific frequency range (based on baud rate)
- Insertion Loss Deviation (ILD): The insertion loss deviation is the algebraic difference between the insertion loss and the fitted attenuation (also known as passband ripple)
- Return Loss (RL): Defined as the magnitude, expressed in decibels, of the differential SDD11 response of the channel
- Insertion Loss to Crosstalk Ratio (ICR): The least mean squares line fit to the ratio of the insertion loss, IL) to the power sum of all forward and reverse differential crosstalk sources (in dB), computed over a specific frequency range (based on baud rate)
- Intra-pair skew: The skew between the two traces in a differential pair
- Lane-lane skew: The skew between lanes that are bundled into a pipe as defined in the backplane profile

For more insight into the signal integrity parameters, see the white paper on Hybricon's website "Signal Integrity - Revving up VPX for 10Gbaud operation" at [http://www.hybricon.com/News/technical\\_papers\\_download.aspx?id=126](http://www.hybricon.com/News/technical_papers_download.aspx?id=126)

VITA 68 defines an end-to-end channel including multi-line coupled plug-in module Tx and Rx pads, vias and traces as well as multi-line coupled backplane traces, mated connectors, and connector via footprints. It also allocates a budget for each parameter to the backplane portion only, which is defined to include the backplane traces, connectors, via footprints on both the backplane and Tx/Rx plug-in module, and short 2mm traces on Tx/Rx plug-in modules to provide a clearly defined compliance point suitable for physical measurement. Based on preliminary signal integrity simulation work performed by Hybricon, an initial signal integrity budget has been established for the backplane portion and this is documented in the VITA 68 draft standard (but this budget needs to be validated by a VITA 68 signal integrity simulation study).

The idea is to precisely define the backplane performance requirements for each baud rate such that any fabric protocol that runs at that rate could be supported with realistic performance requirements for the Tx/Rx plug-in module traces. For example, a 3.125 Gbaud backplane would need to support 3.125 Gbaud SRIO, Ethernet XAUI, or Ethernet 10GBASE-KX4; it would also need to support lower baud rates such as 2.5 Gbaud Gen 1 PCIe. At the end of the day, each fabric protocol needs to operate at a specified bit error rate (BER); at higher rates this requires modeling of the receiver equalization which varies with different protocols. These different fabric protocols might require different performance requirements for the Tx/Rx plug-in module traces (in order to achieve the required bit error rates), but they would all use the same backplane channel.

## **Signal Integrity Simulations**

Because the backplane is the least common denominator for VPX interoperability, the VITA 46 VPX and VITA 68 working groups have agreed that the VITA 68 working group will develop a Signal Integrity Statement of Work (SOW) and will oversee the signal integrity simulation work to finalize the signal integrity budget for the backplane and to define the signal integrity requirements for the VITA 46.3 SRIO, VITA 46.4 PCIe, and VITA 46.6/VITA 46.7 Ethernet VPX “dot specs”. A draft SOW has been developed based on previous efforts in the VITA 46.3 and VITA 46.4 working groups.

## **Latest VITA 68 developments, status**

VITA 68 became a working group within the VITA Standards Organization at the September 2009 meeting. The draft specification and the draft Signal Integrity SOW are just now undergoing their first VITA working group ballot.

Bob Sullivan is Vice President of Technology at Hybricon Corp. ([www.hybricon.com](http://www.hybricon.com)) and is chairperson of VITA 68. For more information on VITA 68, contact Bob at [bobs@hybricon.com](mailto:bobs@hybricon.com).