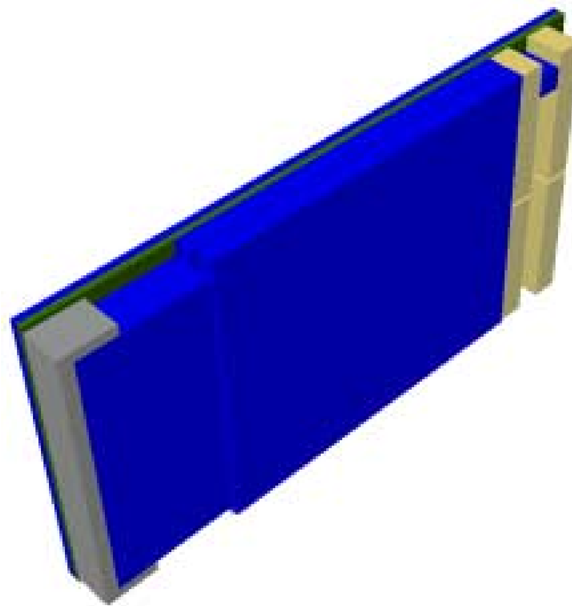
HTF127

Using Mezzanine Card Assemblies:

Power Dissipation & Airflow Evaluation



Prepared By:
Michael R. Palis and Robert C. Sullivan

Revision History Form

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Introduction:

With the functionality of electronics expanding at a rapid pace, as it has over the past twenty to thirty years, various product implementations have been market successes. Form factors such as VME, VME64, VME64x, CompactPCI®, PCI Mezzanine Card (PMC), and Industry Packs (IP) have all been standardized by organizations such as IEEE®, VITA® and PICMG®. In recent years, we have seen rapid growth in product offerings using the Computer Mezzanine Cards (CMC) and PCI Mezzanine Cards (PMC) form factor. A high percentage of new circuit card designs for VME64x and CompactPCI have provisions for supporting at least one (typically PMC) mezzanine module. The flexibility provided by these mezzanine circuit cards allows system integrators to more easily configure solutions with the types and amounts of I/O that they require for their application.

The functionality of CMC/PMC Modules has been recently extended by the ANSI-VITA 32 Processor PMC (PrPMC) standard and further extensions are now being developed by VITA in the VITA 42.x XMC draft standards. PICMG is also developing a new PICMG AMC.x AdvancedMC® series of mezzanine specifications aimed at AdvancedTCA® applications. See Figure 1 for a plot of the PMC/PrPMC/XMC power dissipation values.

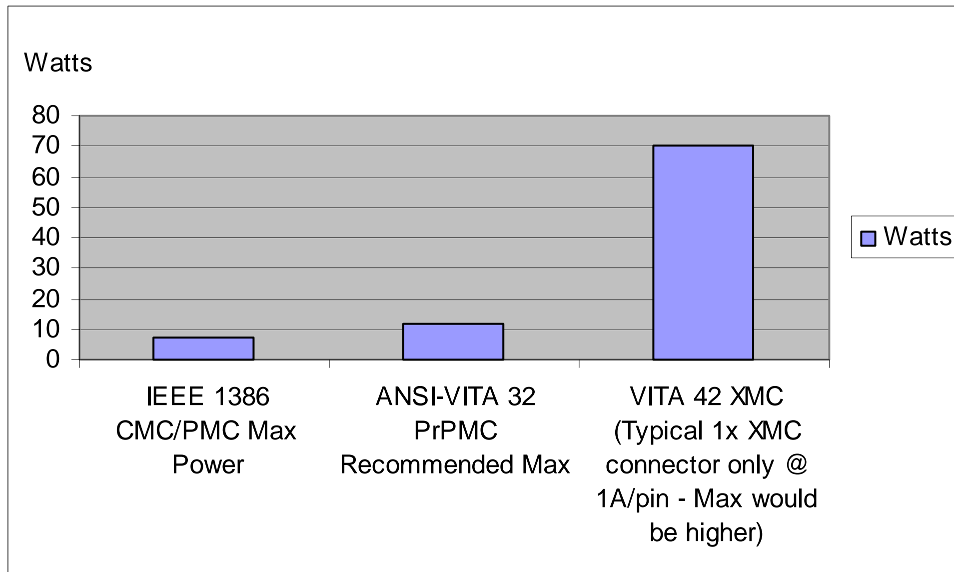

Figure 1: Comparison of Power Dissipation for PMC, PrPMC, and XMC

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These new mezzanine standards target high speed I/O signaling that is needed for modern switch fabrics. High speed I/O often requires higher power, driving the need for supporting higher power dissipations on these mezzanine modules. Higher power modules usually contain large components such as heat sinks, connectors, optical transceivers, and so on. These large components increase the volume utilization[1], which chokes off the air channel, reducing cooling airflow.

The question is, will these higher power dissipations and higher volume utilization cause thermal issues in the system application?

The good news is that there is a rationale for managing the volume utilization and power dissipation in order to avoid thermal problems. Higher power dissipation and volume utilization on mezzanines and carriers can be accomplished by carefully managing these parameters.

Background:

CMC and PMC circuit card assemblies are specified in IEEE Standards, IEEE 1386 and IEEE 1386.1. These standards, even though updated regularly, still allow power dissipation in the range of 7.5 Watts. These power dissipation levels represent device technologies of over twenty years ago, and new devices, architectures and I/O schemes are driving the power dissipation levels, with the new proposed standards to levels approaching 70 Watts as proposed in VITA 42.0 XMC (draft) and PICMG AMC.0 Advanced Mezzanine Card Specification (draft).

These increased power dissipation limits also require more cooling air to keep the electronics cool, but where is the air in applications of CMC/PMC/XMC allowed to go?

Refer to Figure 2 for component envelopes, as defined in IEEE 1386. This topology will be used for subsequent analysis.

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[1] As used in this article, volume utilization is defined as the percentage of the maximum component volume that is actually consumed by the components. The maximum component volume is defined as the maximum component height that is allowed by the PMC/PrPMC/XMC standards multiplied by the board area.

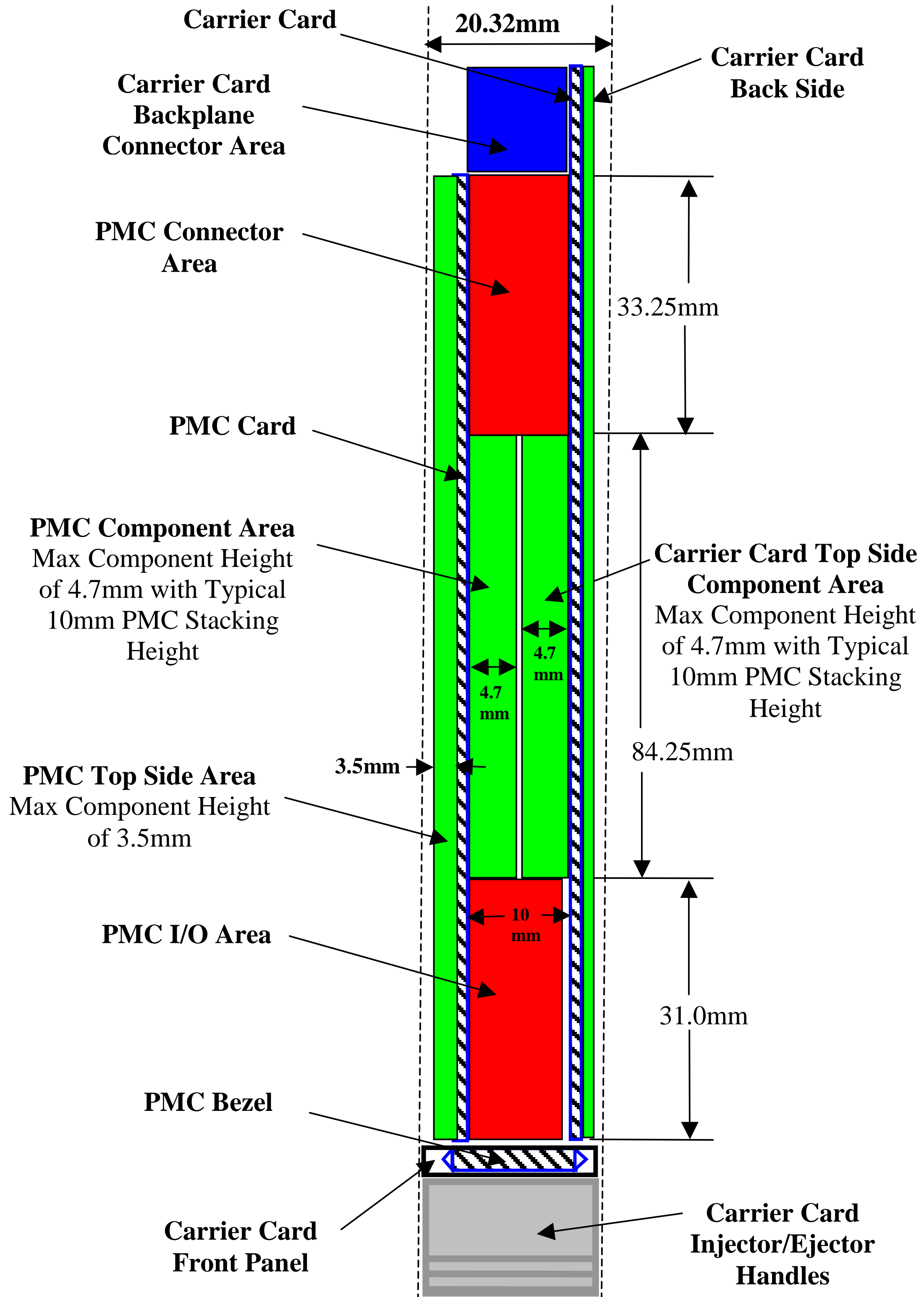


Figure 2: Component areas for PMC mated to Carrier Card on 20.32mm (0.8") pitch

Early implementations of CMC/PMC Modules had high heat dissipation and high height devices installed onto the modules, and were classified as being low profile. These devices were Single Inline Packages (SIP), Dual Inline Packages (DIP) and axial leaded devices and passive wire connections of DB-9, DB-15 and DB-25 connectors. Modern I/O schemes are now active and more complex in their implementation, and include the following examples:

1. Optical Transceivers
2. Giga-Bit Ethernet Connectors
3. High Data Rate Connectors with Active Filtering

These I/O devices consume more volume than the wired technologies of the past and in addition these devices now dissipate power, where the passive connector of the past did not. The additional functionality of the active devices is also represented in large volume packages installed on the Printed Wiring Boards (PWB) and may be in the form of Ball Grid Arrays approaching 50 mm by 50 mm by 10 mm tall.

This all means that modern electronics are dissipating higher power levels into board volumes that are being consumed with these device packages. This has the impact of reducing the volumes within the assemblies where the cooling air needs to flow.

What happens from an airflow perspective as the component envelopes are consumed with high heat and higher volume components? The following questions come to mind:

1. Is the air going to the area that needs maximum airflows?
2. Are the Higher Power Dissipation devices being cooled?
3. Can High Power dissipating devices be placed in areas that facilitate cooling?
4. Is it possible to fully utilize the proposed new higher mezzanine power dissipation limits without causing other thermal problems?

To answer the questions stated above, the Mass Flow Rate Heat Transfer equation is reviewed.

$$Q = C_p * dm/dt * (T_{out} - T_{Ambient}) \text{ (e.q. 1)}$$

Where Q = Total Heat Dissipated in Watts

Cp= The Specific Heat of the Fluid being used.
dm/dt= Mass Flow rate, $=\rho * dV/dt$,
Where dV/dt = volumetric flow rate (CFM) and ρ= fluid density (lb_m/ft^3)

As seen in this equation, the management of temperatures of power dissipating devices is very dependant on the volumetric flow rate in the volume of the device that is dissipating power. The higher the device power dissipation, the higher the volumetric flow rate and incident velocity over the device is required.

Simulation Parameters:

Since the CMC/PMC form factor is widely adopted in industry, and the new, higher power XMC versions are emerging, we chose this form factor for further study.

A model geometry was created in Flotherm® for modeling the maximum space envelope as specified by IEEE 1386 and 1386.1 CMC and PMC standards. This model is shown in Figure 3.

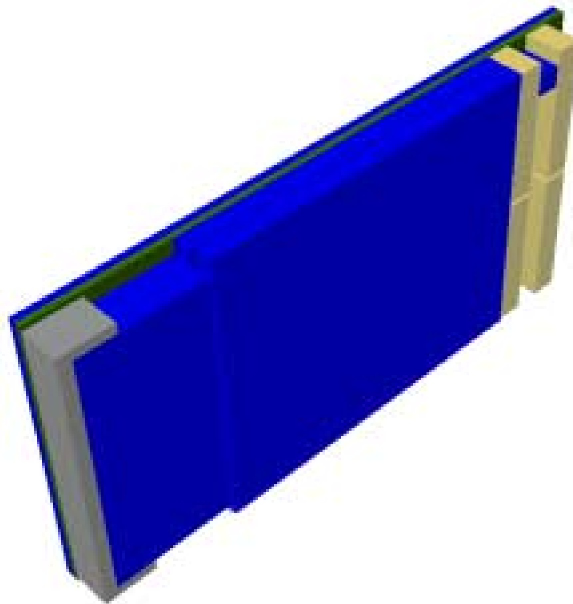


Figure 3: CMC/PMC Module Component Envelope Perspective View

A Flotherm model was setup to simulate a mated CMC/PMC/XMC module and carrier card. Figure 2 shows the definition of the flow regions that were setup in the Flotherm

model. These flow regions were used to track the distribution of the airflow as it travels through the CMC/PMC module and carrier assembly. The I/O is identified in Figure 2 and Figure 3 for completeness, but for this evaluation was set at 100 % blocked to represent the metal front panel and effects of large optical transceivers and connectors that are commonly used in many PMC modules now on the market.

Detailed Results:

Using a wind tunnel model technique in Flotherm, a series of Computational Fluid Dynamics (CFD) analyses were performed at the following environmental conditions:

1. 55º C ambient, representative of a military COTS or telecommunications environment.
2. Mean Sea Level (MSL) conditions[2]

Concentrating on the volume of air available to cool the components, and monitoring the flow rate in the regions defined above, a series of analyses were performed to determine the distribution of the airflow as the component volume utilization is varied from 100% of the component envelope allowed by IEEE 1386 and 1386.1 (CV100) to 20% of the allowed component envelope (CV 20). For example, at a volume utilization of CV100, all components would be at their maximum heights per Figure 2. Refer to Figure 2 for details on these maximum component envelopes.

Figures 4 and 5 show the distribution of the airflow into the PMC and Carrier Board and through the PMC and Carrier Board, for the maximum component volume utilization case (CV100); this is the worst case for airflow. The results of these analyses are tabularized in Table 1.

[2] Mean Sea Level defines the density and pressure of the atmosphere at sea level (zero) altitude and a temperature of 15C, per the U.S. "Standard Atmosphere" tables. Refer to "*U.S. Standard Atmosphere*, 1976" published by the U.S. Government Printing Office, Washington, D.C.

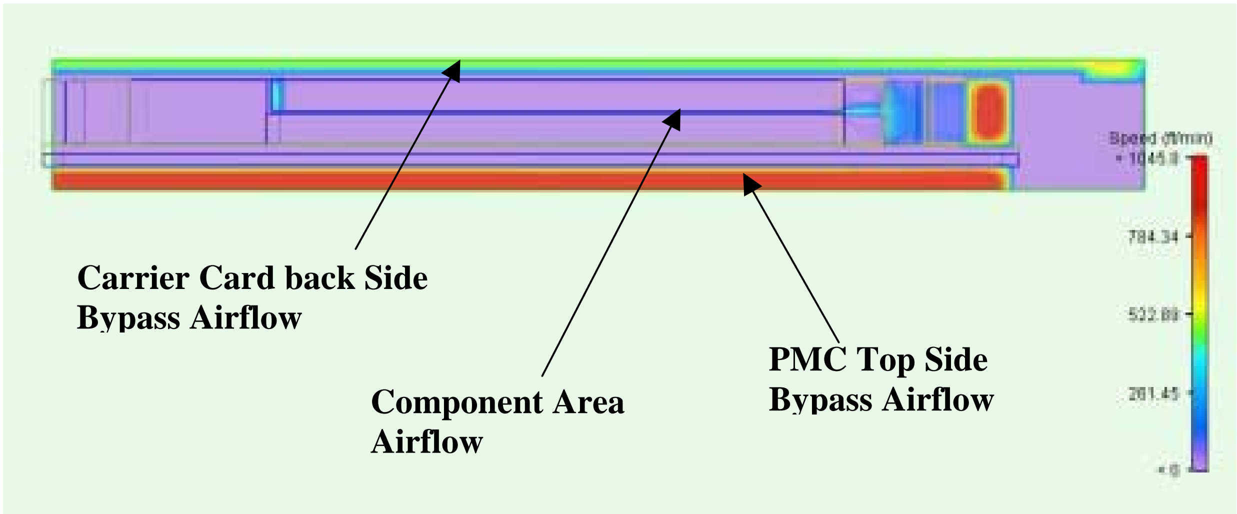


Figure 4: Simulated Intake Airflow For CMC/PMC Module with Maximum Component Volume Utilization (CV100)

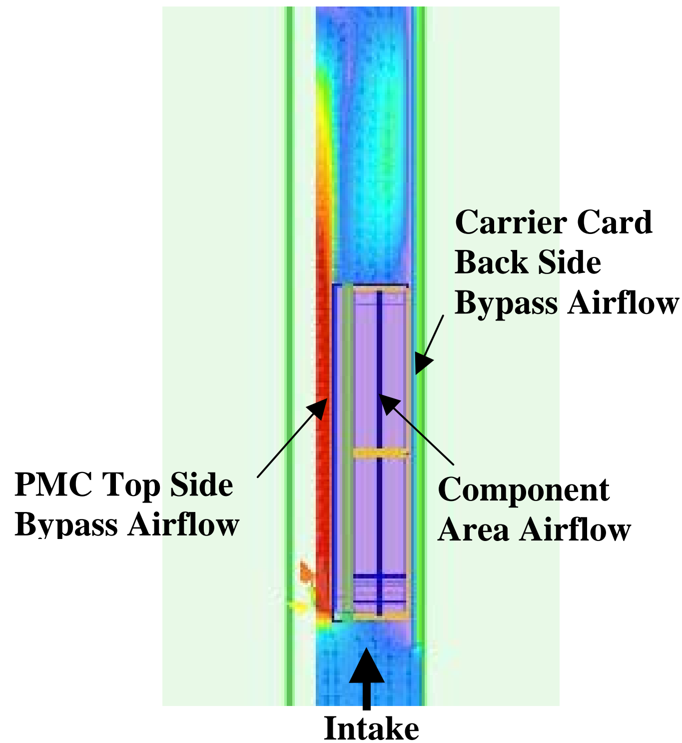


Figure 5: Simulated Side View Airflow For CMC/PMC Module with Maximum Component Volume Utilization (CV100)

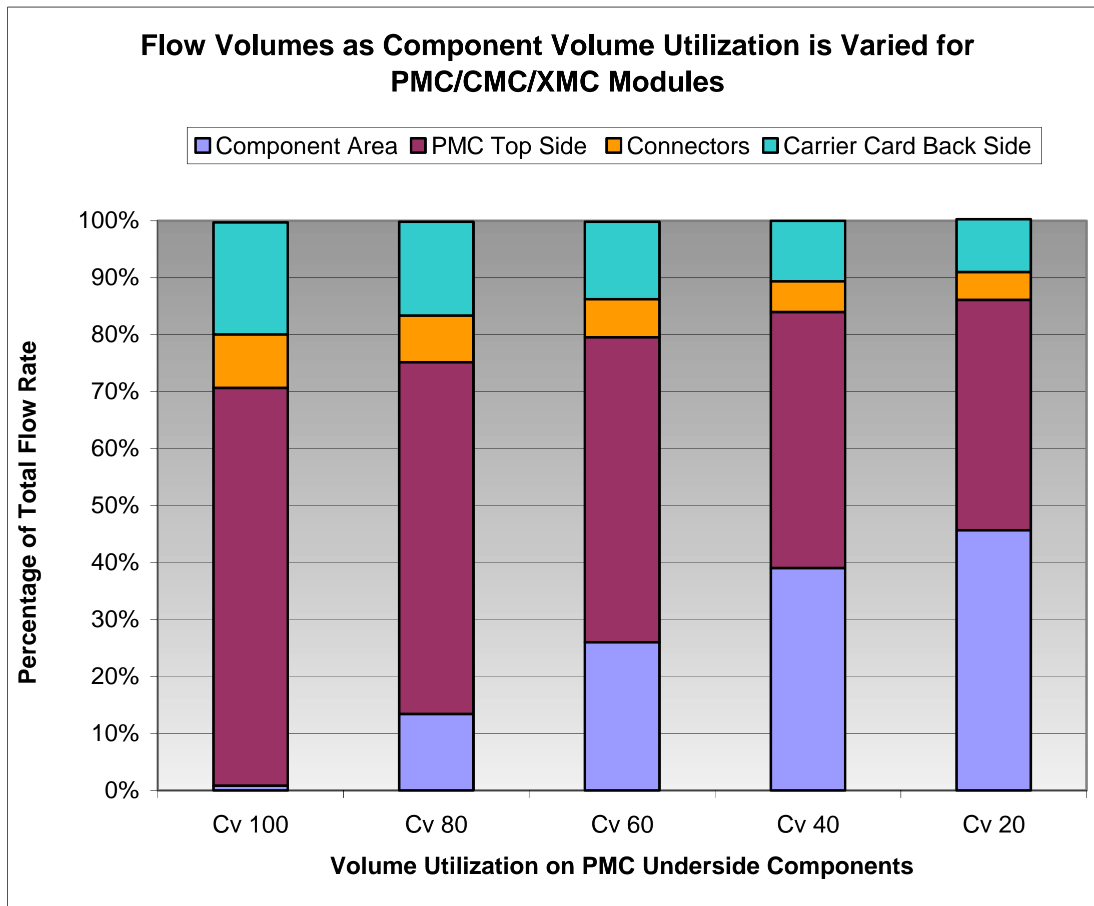


Table 1: PMC/CMC/XMC Flow Volumes

As expected, Table 1 shows that the percentage of the airflow that is actually flowing in the component area between the CMC/PMC/XMC mezzanine module and the carrier card is strongly dependent on the component volume utilization. However, you may be surprised to learn just how little air is actually flowing in the component area. From the results in Table 1, we are able to make some observations as follows:

1. As the component volume utilization is lowered from the specification maximum envelope (CV100) to twenty percent of this maximum envelope (CV20), the airflow patterns through the module vary dramatically. The flow through the various regions changes as the component volume utilization changes, with a large air bypass over the PMC top side.
2. Active PMC carrier cards, such as single board computers, often specify minimum flow rates in order to cool the carrier card itself. For example, the Motorola® MVME 5500 has (2) PMC sites, and specifies 400 LFM of cooling. Even for low

component volume utilizations (CV20), less than 50% of the available air volumes are actually cooling the components placed in the component area. Even at (CV20), this has the impact of needing more than double the carrier card's required flow rate into the slot in order to deliver the required airflow to the component area. This gets much worse as the component volume utilization is increased.

3. For all component volume utilizations above 20% (CV20), the airflow in the component area (where we typically want the air to flow) is less than the airflow bypass over the PMC top side.
4. At maximum component volume utilization (CV100), the airflow in the component area between the CMC/PMC/XMC mezzanine module and the carrier card is only 1% of the total airflow through the slot.
5. High power XMC mezzanine modules must be designed to conduct heat to the XMC top side, and take advantage of the significantly higher XMC top side bypass airflow to cool the module. This can be done using techniques such as solder-filled vias, together with very low profile XMC top side heat sinks (keeping in mind that the PMC top side component height is limited to 3.5mm maximum). This is even more critical for high component volume utilizations, since the airflow in the component area is very low for these designs.
6. Even low power CMC/PMC designs with high component volume utilizations should be designed to conduct heat to the XMC top side, and take advantage of the significantly higher XMC top side bypass airflow to cool the module.

Another impact of higher component volume utilization is the effect that this has on the so-called P-Q curve (pressure vs. mass flow) of the carrier and CMC/PMC/XMC modules. As the component volume utilization increases, the P-Q curve also increases, making it more difficult to move the air. P-Q curves for various volume utilizations are shown in Figure 5.

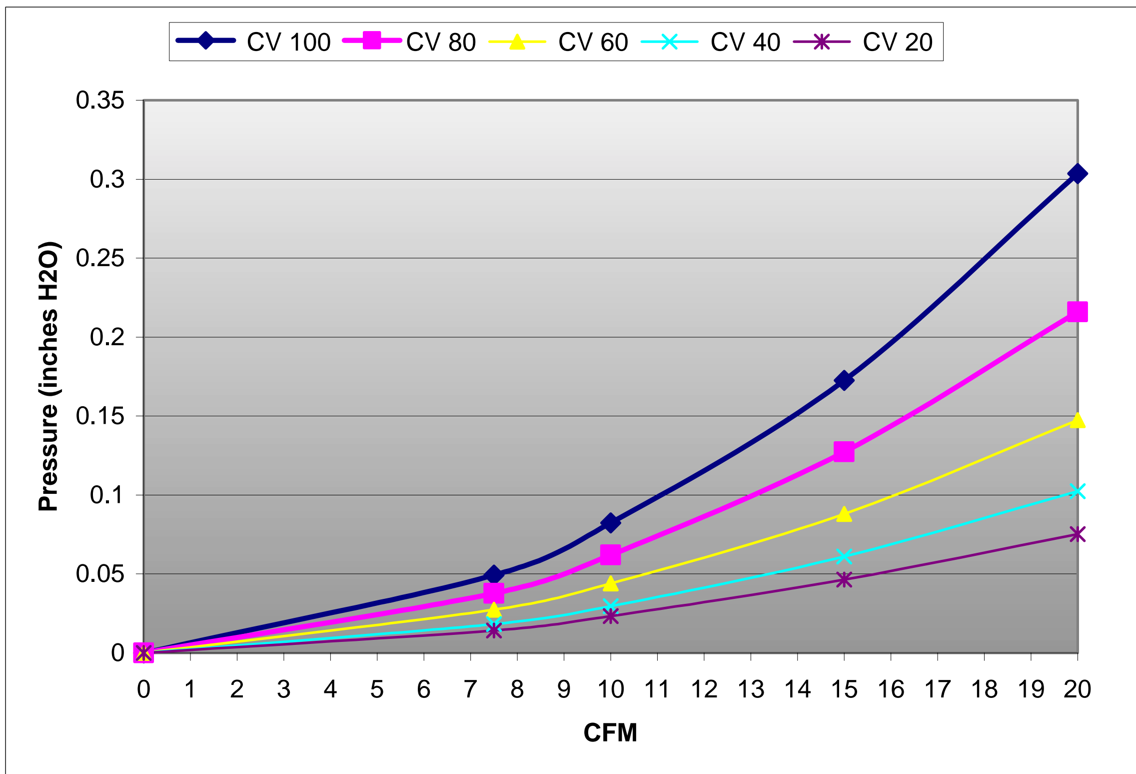


Figure 6: CMC/PMC/XMC Module P-Q Curve vs. Volume Utilization

The impact of the increased pressure, as shown in Figure 5, may have a system impact of requiring higher capacity fans to over come this higher pressure (resistance to flow) and can lead to myriad system level tradeoffs that can impact the following:

1. Air movers (fans, blowers)
2. System Size
3. Total Input System Power
4. Acoustic Noise

Conclusions and Recommendations:

We arrived at the following conclusions and recommendations for system architects and hardware implementers who are selecting mezzanine modules for a system level application:

1. As more components are installed in the component area, the volume of air that cools the components is reduced and may cause thermal management problems, so it is important to review the topologies of the Carrier Cards and installed modules

to ensure that the air is actually cooling the higher power and/or thermally sensitive devices.

2. A high percentage of the air is bypassing the component area of the CMC/PMC/XMC Modules. Techniques such as thermal vias and low profile PMC top side heat sinks should be used for higher power modules or modules with high component volume utilizations.
3. Great care is required when using high power mezzanine modules such as XMC modules, in order to avoid assembly and system level thermal problems.
4. Even if a low power CMC/PMC/XMC module is being used, if it has a high volume utilization (tall components), then it could cause thermal problems, particularly if it is installed on a CMC/PMC/XMC site on an active carrier card such as a single board computer. This is because it can severely restrict the airflow to the component area; this airflow may be needed to cool hot components on the active carrier card.

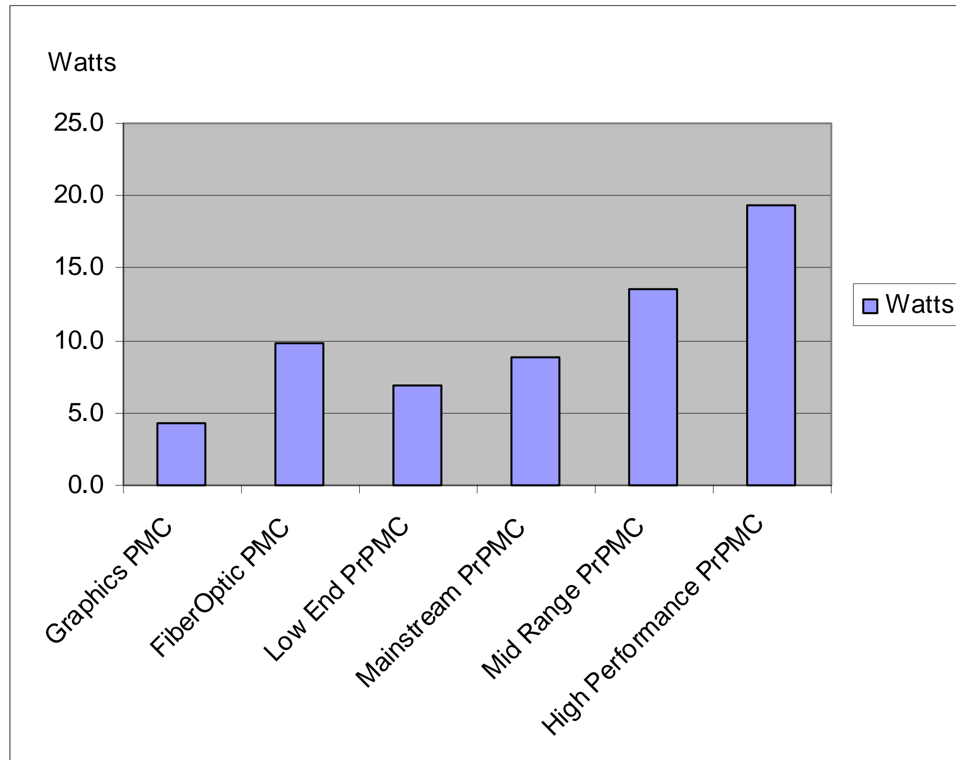
Sidebar – Active Switch Fabrics and Power Dissipation:

The emerging VITA 42.x XMC standards and PICMG AMC.x specifications are both aimed at very high-speed serial switch fabric applications. Initial applications utilize InfiniBand, Ethernet/XAUI, Serial RapidIO, and PCI Express, with signaling rates typically running at 2.5 Gbps – 3.125 Gbps per pair.

Mezzanine cards that are designed to support these very high signaling rates will tend to consume more power than their lower speed PCI-interfaced brethren.

1. Interfacing to these very high-speed serial switch fabrics requires high on-chip clock rates and sophisticated clock recovery circuitry, both of which tend to drive power consumption upward.
2. Mezzanine card performance and functionality will naturally be increased to take advantage of the bandwidth available.
3. Performance of the external interfaces (e.g. optical transceivers) will increase as well to take advantage of the bandwidth available.

4. See the Sidebar Figure for a sample of typical power dissipation for existing PMC and PrPMC products. As you can see, a number of these are already pushing the envelope on power dissipation. I predict that XMC and AdvancedMC mezzanine power dissipation values will go much higher, making the system integrator's job a lot harder.



Sidebar Figure: PMC/PrPMC Existing Product Typical Power Dissipation Values