

Signal Integrity – performance and reliability for next-generation military rugged embedded computing applications

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Background

Historically, many military rugged embedded computing applications have utilized multi-drop parallel bus architectures, notably VME[™], VME64x[™], and CompactPCI[™]. These multi-drop parallel bus architectures operate at relatively slow clock and data rates ≤ 66 MHz. Signal Integrity performance is guaranteed by simple compliance rules for impedances, trace lengths, and terminations and the like as defined in the industry standards.

Today's modern embedded computing standards, notably OpenVPX[™], VPX[™], VXS[™], and MicroTCA[™], are based on high speed serial differential-pair point-to-point connections often referred to as switched fabrics. Today, these serial differential-pair point-to-point connections operate at 1 Gbps – 3.125 Gbps per differential-pair, and these data rates will increase in the near future. Signal Integrity for this type of application is significantly more complex, with 3-dimensional geometries in printed circuit boards and circuit board dielectric materials now playing an important role.

What is important to guarantee reliable operation?

In order to guarantee reliable operation at these high speeds, several elements of the product need to be considered:

1. Type of serial fabric and data rate (Serial RapidIO, PCIe, etc.)
2. Serial fabric data rate (3.125 Gbps, 2.5 Gbps, etc.)
3. Module Tx device performance characteristics (drive strength, Tx equalization, jitter, etc.)
4. Module Tx printed circuit board trace and dielectric characteristics
5. Module Tx printed circuit board connector via characteristics and launch layer
6. Backplane printed circuit board connector via characteristics and launch layer
7. Backplane printed circuit board trace and dielectric characteristics
8. Module Rx printed circuit board connector via characteristics and launch layer
9. Module Rx printed circuit board trace and dielectric characteristics, i.e. loss characteristics
10. Module Rx device performance characteristics (sensitivity, equalization, jitter sensitivity, etc.)

[™] VME, VME64x, OpenVPX, VPX, VXS are trademarks of VITA; CompactPCI, MicroTCA are trademarks of PICMG

At the end of the day, what's important is to have a low bit error rate (BER) conforming to the standard. All of these elements of the design play a part in determining the performance of the system, in terms of the eye openings and resultant BER.

Often, the underlying serial fabric standards are not fully specified for use across a backplane, so serial transceiver device characteristics become critical to reliable operation.

Focusing on **OpenVPX**[™]

OpenVPX is emerging as the leading standard for next-generation military rugged embedded computing applications. Let's take a look at how some of the OpenVPX and VPX standards address Signal Integrity today.

ANSI/VITA 46.0 VPX Baseline Standard

The ANSI/VITA 46.0 VPX Baseline Standard sets general guidelines for high speed differential point-to-point fabric connections, recommending that backplanes should be designed to support a signaling rate of at least 3.125 Gbps.

This is necessary, but not sufficient to guarantee performance. There are no criteria for goodness on the module or the backplane.

VITA 46.3 Serial RapidIO on VPX

The VITA 46.3 Serial RapidIO on VPX draft 0.9 sets general guidelines for SRIO differential point-to-point fabric connections, requiring compliance with the RapidIO Interconnect Specification Part 6: 1x/4x LP-Serial Physical Layer Specification, Revision 1.3 for the Serial RapidIO "long run" transmitter as well as the receiver; however, performance of the interconnect on the modules and the backplane is not specified.

This is necessary, but not sufficient to guarantee performance, as it primarily addresses minimum transmitter and receiver characteristics. Key items that are not addressed include:

- Transmitter pre-emphasis is not specified (this is critical for minimizing Inter-Symbol Inference with long trace lengths as for VPX).
- There is no budget allocating key parameters such as loss and crosstalk to the module and backplane performance.

Key items that will dramatically impact performance include the following (for module Tx, module Rx, backplane):

- Insertion Loss – determined by dielectric type, trace geometry, trace length, 3D pad & via resonances characteristics
- Crosstalk – determined by trace coupling & via 3D coupling

The SRIO specification allows a worst case loss of 12dB (derived from 800mV min driver amplitude and 200mV min receiver amplitude).

- There is no budget allocating the signal integrity contribution between the modules and the backplane.
- How much of this is for the module Tx path, module Rx path, and backplane path?
 - How a module is designed determines how much of the total loss and crosstalk budget is consumed by the module
 - How a backplane is designed determines how much of the total loss and crosstalk budget is consumed by the backplane
 - If different assumptions were made on the allocation of this budget, different modules and backplanes may not work together in a system

Hybricon recently spearheaded the formation of the VITA 68 Compliance Channel Working Group, which is currently working to tighten this up and set some guidelines for the signal integrity performance of modules and backplanes. Meanwhile, how do you know that your modules and backplane will work together?

Hybricon’s approach for standard VPX and **OpenVPX™** backplanes

Knowing that the VPX standards do not set guidelines for the signal integrity performance of individual elements in the system, Hybricon has adopted a conservative approach to the design of our standard backplanes.

While some other suppliers utilize inexpensive dielectric materials (PCB FR-4 or equivalent), Hybricon utilizes a low loss dielectric material (Nelco 400-13) for our standard backplanes. Hybricon also back-drills top-launch connector vias to minimize via resonances which can seriously degrade performance at 3.125 Gbps and above. We do this to provide the best possible backplane performance while maintaining a reasonable cost. This minimizes the risk of signal integrity problems with a range of suppliers’ VPX modules.



Figure 2 Insertion loss of end-to-end path – 4” modules and 12” backplane

Figure 1 above shows the simulated end-to-end insertion loss of the entire path with a typical well-designed modules using 4” Tx 4-mil 0.5-oz traces and 4” Rx 4-mil 0.5-oz traces using low-loss dielectric along with Hybricon’s backplane or a competitive FR-4 backplane with 12” backplane traces.

At 3.125 Gbps with well-designed Nelco 4000-13 Tx/Rx modules, about half of the total insertion loss is due to the Tx/Rx modules themselves, leaving half for the backplane. If the Tx/Rx modules have longer traces or use a poorer dielectric, they will have higher losses. Similarly, if the backplane has longer traces, does not backdrill top launch vias, or use a poorer dielectric, it will have higher losses.

OK, so what does this do to the eye diagrams?

We simulated a typical VPX fabric connection; see Figure 2 below:

- Uses statistical simulation technique based on the channel pulse response
- Uses behavioral driver and receiver
- Driver output level: +/-500mV (relatively weak but realistic)
- Driver de-emphasis: optimized for each test case
- 1% random jitter added at the receiver
- Crosstalk was not modeled
- Virtex5 FXT TX and RX Package Models included
- Module traces: 4”, Backplane traces: 12”
- 3.125Gbps worst-case 8b/10b encoded PRBS stimulus
- Compare 4 scenarios:
 - Nelco 4000-13 dielectric, best case (backdrilled) and worst-case via stubs
 - FR4 dielectric, best-case (backdrilled) and worst case via stubs

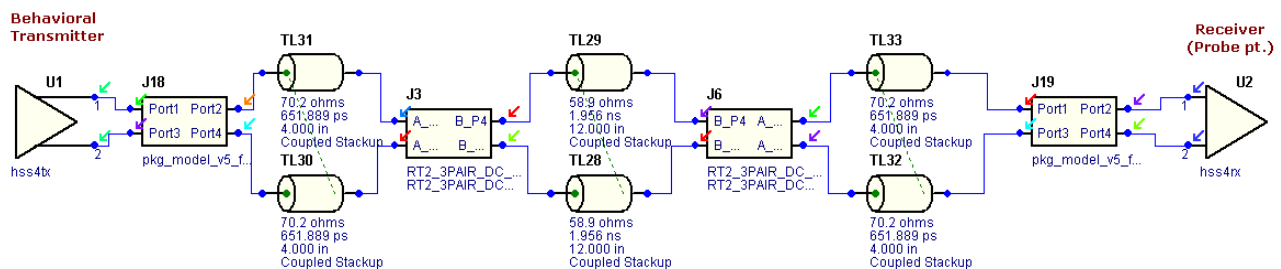


Figure 2 Simulated end-to-end path for eye diagrams

Refer to Figure 3 – Figure 6 for comparative eye diagrams.

Referring to Figure 3 below, it can be readily seen that the backdrilled Nelco 4000-13 backplane in Figure 3 meets the SRIO eye mask. The Eye Height is 264mV which meets the SRIO eye mask and BER $10E^{-12}$ contour (inner red line on the eye diagram). The Eye Width @ $10E^{-12}$ BER is 0.915UI.

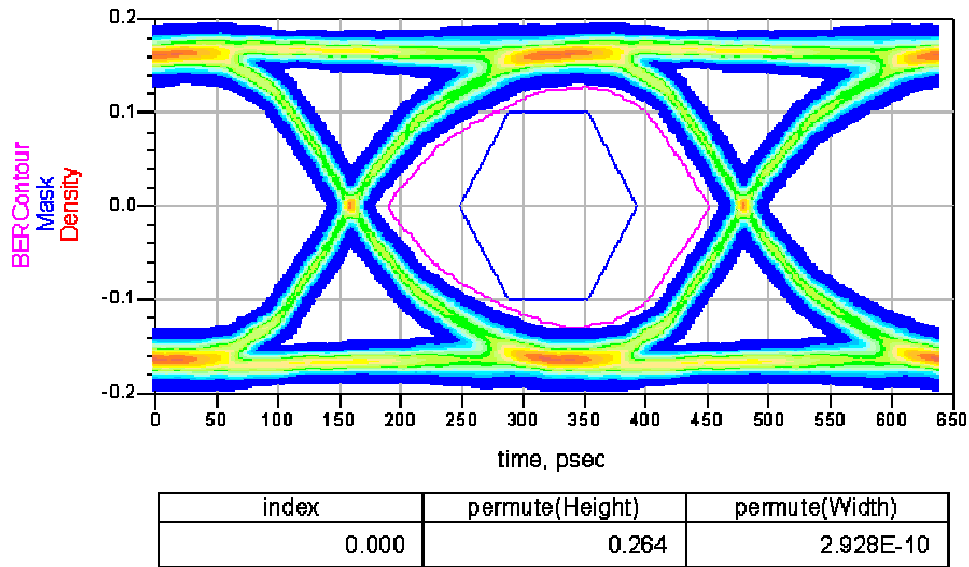


Figure 3 Simulated eye diagram for Nelco 4000-13 without backdrill

Referring to Figure 4 below, it can be readily seen that the Nelco 4000-13 backplane without backdrill in Figure 4 meets the SRIO eye mask. The eye height is 237mV – meets eye mask but is marginal at BER $10E^{-12}$ contour (inner red line on the eye diagram). The eye width @ $10E^{-12}$ BER is 0.875UI. With longer traces on the backplane or the plug-in module, this would not work reliably.

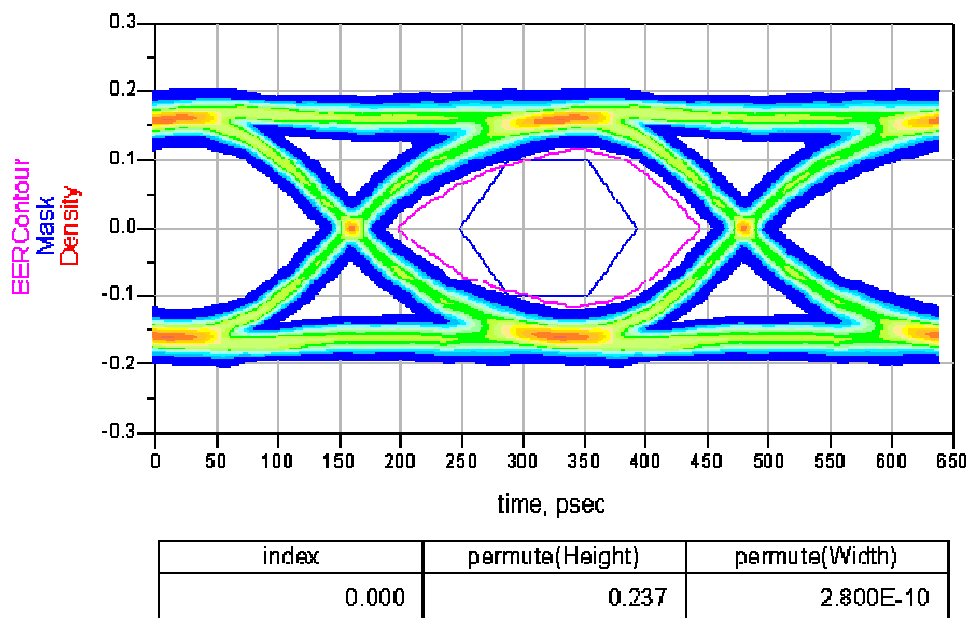


Figure 4 Simulated eye diagram for Nelco 4000-13 without backdrill

Referring to Figure 5 below, it can be readily seen that the backdrilled FR-4 backplane in Figure 5 is marginal vs. the SRIO eye mask. The Eye Height is 209mV which is marginal for the eye mask but violates BER $10E^{-12}$ contour (inner red line on the eye diagram). The Eye Width @ $10E^{-12}$ BER is 0.895UI. This backplane would yield high bit error rates.

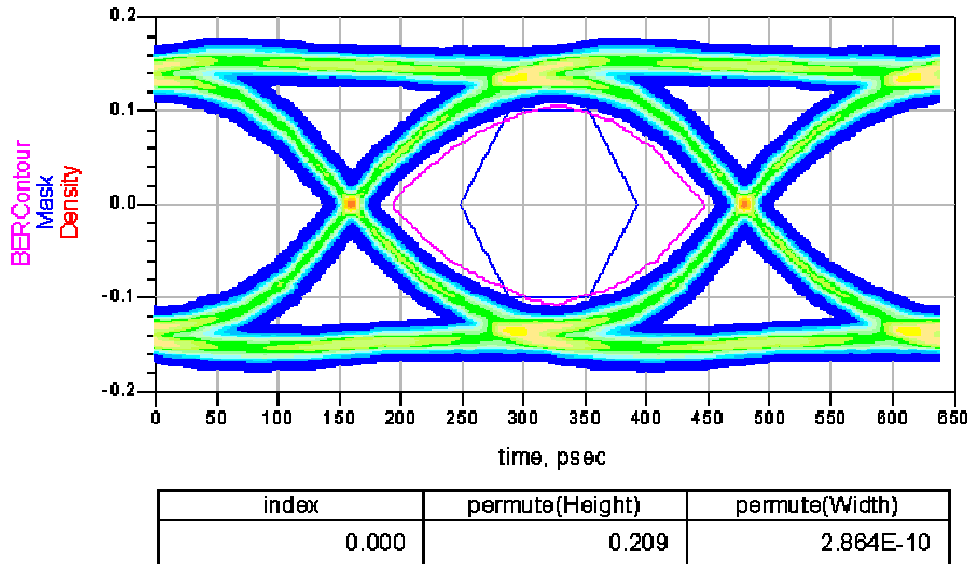


Figure 5 Simulated eye diagram for FR-4 with backdrill

Referring to Figure 6 below, it can be readily seen that the non-backdrilled FR-4 backplane in Figure 6 fails to meet the SRIO eye mask. The Eye Height is 194mV, which is an SRIO MASK VIOLATION. It also clearly violates the BER $10E^{-12}$ contour (inner red line on the eye diagram). This backplane would yield very high bit error rates.

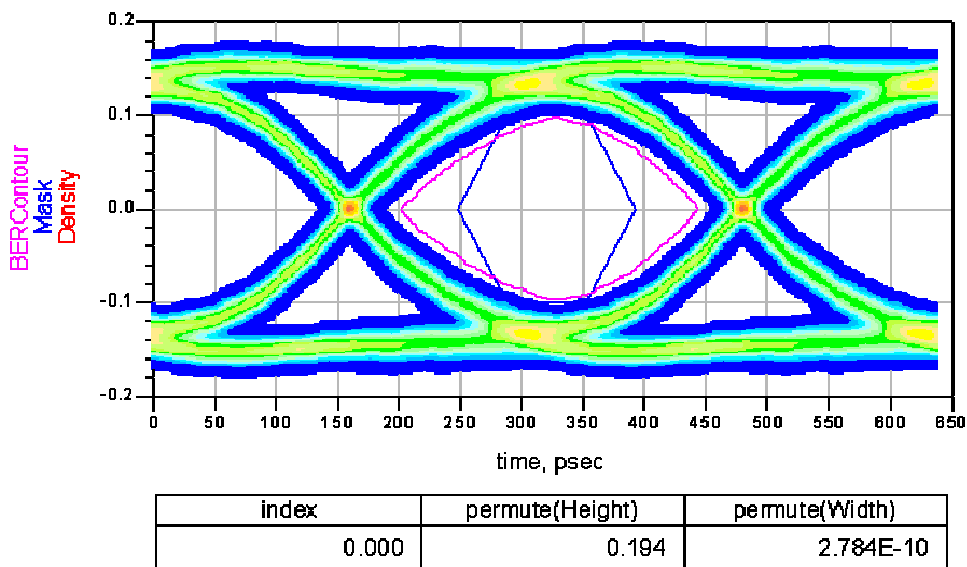


Figure 6 Simulated eye diagram for FR-4 without backdrill

Even with a 12” long backplane, the only one of these cases that will meet a $10E^{-12}$ BER is the backdrilled Nelco 4000-13 backplane. These other backplane designs may marginally work with stronger SRIO transmitters, but the weaker transmitters (which still comply with the SRIO specification) will have problems with lower performance backplane designs. At higher speeds, they won’t work at all.

Signal integrity performance for **OpenVPX™** in military programs – a critical success factor

Because the current OpenVPX and VPX standards do not allocate the budget nor set guidelines for the signal integrity performance of modules and backplanes, signal integrity simulations for the complete end-to-end path are a critical success factor for military programs. Hybricon routinely performs these signal integrity studies to ensure that the specific VPX modules that are used for a particular application will provide adequate margin over worst-case operating conditions with Hybricon’s backplane (which is often a program-specific custom or modified design).

Since we know that many U.S. military programs have ITAR restrictions, all of our signal integrity simulation work is done at Hybricon’s facilities in the USA, in compliance with ITAR restrictions.

For development backplanes and systems, Hybricon has adopted a conservative approach to the design of our standard backplanes. Hybricon utilizes a low loss dielectric material (Nelco 400-13) for our standard backplanes, and back-drills top-launch connector vias to minimize via resonances which can seriously degrade performance at 3.125 Gbps and above. As can be seen above, lower performance backplanes run the risk of signal integrity problems, and above all we want to ensure that our backplanes work with any reputable supplier’s VPX modules.

Led by Hybricon, the VITA Standards Organization is in the process of defining a VPX compliance channel standard, VITA 68. VITA 68 will establish the criteria for signal integrity compliance of VPX backplanes and plug-in modules. Once completed, VITA 68 will provide the roadmap for improved interoperability. This is absolutely essential as we rev up the baud rates to 5gig and beyond.

Working with Hybricon

Hybricon doesn’t just make backplanes and chassis! We can provide a system view and assist with tradeoffs early in your design planning phase to ensure that your OpenVPX program comes off without a hitch. Along with Thermal Management, Signal Integrity is one of the most critical success factors for OpenVPX-based programs.