

VITA 68 allows a common backplane design for multiple fabric protocols

By Bob Sullivan

VITA 68 (VPX Compliance Channel) defines a VITA 46 (VPX) compliance channel based on the channel performance methodology and metrics used in IEEE 802.3-2008 for 1000BASE-KX, 10GBASE-KX4, and 10GBASE-KR for up to 10.3 Gbaud per pair.

This methodology is comprehensive and defines a number of frequency domain channel parameters that can be adapted to the PCI Express and Serial RapidIO Gen 1 and Gen 2 baud rates. Key channel parameters are:

- Insertion Loss (IL)
- Fitted Attenuation (FA)
- Insertion Loss Deviation (ILD)
- Return Loss (RL)
- Insertion Loss to Crosstalk Ratio (ICR)
- Intra-pair skew
- Lane-lane skew

VITA 68 defines an end-to-end channel including multi-line coupled plug-in module Tx and Rx pads, vias, and traces as well as multilane coupled backplane traces, mated connectors, and connector via footprints. It also allocates a budget for each parameter to the backplane portion only. Based on preliminary signal integrity simulation work performed by Hybricon, an initial signal integrity budget has been established for the backplane portion. This is documented in the VITA 68 draft standard.

The idea is to precisely define the backplane performance requirements for each baud rate such that any fabric protocol that runs at that rate could be supported. For example, a 3.125 Gbaud backplane would need to support 3.125 Gbaud Serial RapidIO, Ethernet XAUI, or 10 GBASE-KX4, plus lower baud rates such as 2.5 Gbaud PCI Express. Each fabric protocol needs to operate at a specified Bit Error Rate (BER); at higher rates this requires modeling the receiver equalization, which varies with different protocols. These different fabric protocols would all use the same backplane channel.

Signal integrity simulations

Since the backplane is the least common denominator for VPX interoperability, the VITA 46 and VITA 68 working groups have agreed that the VITA 68 working group will develop a signal integrity Statement of Work (SOW). The working group will oversee the signal integrity simulation work to finalize the signal integrity budget for the backplane and to define the signal integrity requirements for the VITA 46.3 Serial RapidIO, VITA 46.4 PCI Express, and VITA 46.6/VITA 46.7 Ethernet VPX dot-specs. A draft SOW has been developed based on previous efforts in the VITA 46.3 and VITA 46.4 working groups.

Latest VITA 68 developments

VITA 68 became a working group within the VITA Standards Organization (VSO) at the September 2009 meeting. The draft

specification and the draft signal integrity SOW are just now undergoing their first VITA working group ballot.

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